

In the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

1           1. (Previously Amended) A method for emulation communications  
2 via a test data input port and boundary-scan architecture providing  
3 serial access to a serial connection of a plurality of registers  
4 disposed in a plurality of modules, each of the plurality of  
5 modules including at least one of the plurality of registers,  
6 comprising the steps of:

7           selecting for communication one of said plurality of modules,  
8 nonselected modules being nonresponsive to data on said serial  
9 connection;

10          supplying to the test data input port for communication to the  
11 boundary-scan architecture a serial signal having a number of bits  
12 greater in number than a number of bits of the serial connection of  
13 the plurality of registers, each bit of said serial signal having a  
14 first digital state;

15          following supply of said serial signal, supplying to the test  
16 data input port for communication to the boundary-scan architecture  
17 a single start bit having a second digital state opposite to said  
18 first digital state followed by a predetermined number of data  
19 bits;

20          at said selected module detecting said single start bit within  
21 the boundary-scan architecture and storing said predetermined  
22 number of data bits.

1           2. (Original) The method of claim 1, wherein:

2           said step of storing said predetermined number of data bits  
3 consists of storing said predetermined number of data bits in a  
4 program visible data register.

1        3. (Original) The method of claim 1, further comprising:  
2        at said selected module, interpreting said predetermined  
3        number of data bits as an instruction and performing a function  
4        corresponding to said instruction.

1        4. (Previously Amended) The method of claim 1, wherein the  
2        boundary-scan architecture includes a test data output port  
3        following a last of the serial connection of registers, the method  
4        further comprising:  
5        at said selected module, identifying a predetermined number of  
6        data bits to be transmitted, supplying to following registers in  
7        the serial connection of the plurality of registers a single start  
8        bit having a second digital state opposite to said first digital  
9        state followed by said identified predetermined number of data bits  
10       to be transmitted.

1        5. (Previously Amended) The method of claim 1, wherein:  
2        said first digital state is 1; and  
3        said second digital state is 0.

1        6. (Currently Amended) A digital electronic module  
2        comprising:  
3        a serial scan path having a serial input and a serial output  
4        and connecting through a plurality of data registers within the  
5        digital electronic module;  
6        a start bit detector having a start bit detector input, a  
7        start bit detector output and an alternative data output, said  
8        start bit detector monitoring serial data received at said start  
9        bit detector input and coupling serial data received at said start  
10       bit detector input to said start bit detector output except upon  
11       detection of a number of serial bits ~~greater than a first~~  
12       ~~predetermined number~~ having a first digital state followed by a

13 single start bit having a second digital state opposite to said  
14 first digital state coupling a second predetermined number of bits  
15 of serial data received at said start bit detector input to said  
16 alternative data output;

17 an alternative data input register connected to said  
18 alternative data output of said start bit detector for receiving  
19 and storing data output by said start bit detector on said  
20 alternative data output;

21 an input switch having a serial test data input and a first  
22 mode input, said input switch connecting said serial test data  
23 input to said serial ~~data~~ input of said serial scan path upon  
24 receiving a serial scan path mode signal at said first mode input  
25 and connecting said serial test data input to said ~~serial-data~~  
26 start bit detector input of said start bit detector upon receiving  
27 an alternate data transfer protocol mode signal at said first mode  
28 input; and

29 an output switch having a test data output and a second mode  
30 input, said output switch connecting said serial ~~data~~ output of  
31 said serial scan path to said test data output upon receiving said  
32 serial scan path mode signal on said second mode input and  
33 connecting said ~~serial-data~~ start bit detector output of said start  
34 bit detector to said test data output upon receiving said alternate  
35 data transfer protocol mode signal at said second mode input.

1 7. (Previously Amended) The digital electronic module of  
2 claim 6, wherein:

3 said first digital state is 1; and

4 said second digital state is 0.

1 8. (Currently Added) The digital electronic module of claim  
2 6, further comprising:

3 a bypass path connecting said input switch and said output  
4 switch;  
5 said input switch further connecting said serial test data  
6 input to said bypass path upon receiving a bypass path mode signal  
7 at said first mode input; and  
8 said output switch further connecting said bypass path to said  
9 test data output upon receiving said bypass path mode signal at  
10 said second mode input.

1 9. (Previously Added) The digital electronic module of claim  
2 6, further comprising:  
3 a digital circuit connected to said alternative data input  
4 register operable to employ data stored in said alternative data  
5 input register.

1 10. (Previously Added) The digital electronic module of claim  
2 9, wherein:  
3 said digital circuit includes a programmable digital processor  
4 core.

1 11. (Previously Added) The digital electronic module of claim  
2 10, wherein:  
3 said programmable digital processor core employs data stored  
4 in said alternative data input register as an instruction  
5 controlling execution by said programmable digital processor core.

1 12. (Currently Amended) The digital electronic module of  
2 claim 9, further comprising:  
3 an alternative data output register connected to said digital  
4 circuit storing data specified by said digital circuit;  
5 a start bit generator connected to said alternative data  
6 output register and said output switch, said start bit generator

7 generating a start bit having said second digital state followed by  
8 a predetermined number of bits of output data stored in said  
9 alternative data output register; and  
10 said output switch further connecting said start bit and said  
11 predetermined number of bits of output data stored in said  
12 alternative data output register to said test data output upon  
13 receiving a data transmission mode signal at said second mode  
14 input.